Changes Approved 3/17/05 JH

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IN THE SPECIFICATION:

Please amend the specification as follows:

(1) The paragraph from page 4, line 16 to page 5, line 1 has been amended as follows:

The time shift circuit is especially useful for an AC parametric test. In such an application, the time shift circuit of the present invention is comprised of a counter for transferring delay value data in a normal mode and incrementing the delay value data in an AC parametric measurement mode to determine a delay timing of a portion of the test pattern applied to a device under test where a mode selection signal selects either the normal mode or the AC parametric measurement mode, a vernier delay unit for producing timing vernier data based on programmed delay data prepared in the semiconductor test system and the delay value data received from the counter, a timing generator for generating a timing edge for the specific portion of the test pattern based on the timing vernier data from the vernier delay unit, means for ~~stroking~~ strobing an output signal of the device under test at the timing edge from the timing generator, and a strobe recovery circuit for determining pass or fail status of the output signal of the device under test and producing a fail signal when the output signal fails.

(2) The paragraph from page 5, line 2 to page 5, line 6 has been amended as follows:

The fail signal is provided to the counter during the AC parametric measurement mode to increment the delay value data, thereby continuously shifting the timing edge for ~~stroking~~ strobing the output signal of the device under test until a change of state in the output signal is detected.

(3) The paragraph from page 5, line 18 to page 5, line 20 has been amended as follows:

Figure 4A and 4B are timing charts showing example of delay timings created in the vernier delay unit in the time shift circuit in the present invention.

(4) The paragraph from page 6, line 15 to page 6, line 25 has been amended as follows:

The vernier delay unit 14 receives a clock, a vernier enable command signal and vernier data (ex. 6-bit or [5:0]) from, for example, a pattern memory (not shown) programmed prior to the test. The vernier delay unit 14 also ~~receive~~ receives delay value data (ex. 8-bit or [7:0]) from the multiplexer 12. The vernier delay unit 14 provides a vernier enable command and timing vernier data (6-bit or [5:0]) to the timing generator 16. The timing generator 16 generates timing edges based on the clock and the timing vernier data from the vernier delay unit 14 when the vernier enable command signal is valid (ex. high).

(5) The paragraph from page 7, line 20 to page 7, line 25 has been amended as follows:

The two delay values, the delay value data A [7:0] and the delay value data B [7:0], are pre-determined by the user before the start of the test. These values are used by controlling the shift command signal on-the-fly during the testing. A user may also use programmable counters or test patterns to control the shift command signal.

(6) The paragraph from page 7, line 26 to page 7, line 32 has been amended as follows:

It should be noted that any field width can be used for the vernier data, delay value data A and delay value data B, in other words, the values shown in Figure 3 are just one implementation done by the assignee. The use of the dynamic shift feature allows time shifting without changing the data in the pattern memory or without repeatedly generating the test patterns.

(7) The paragraph from page 7, line 33 to page 8, line 10 has been amended as follows:

The concept described above allows a ~~constant~~ continuous time shift based upon the delay value data. In actual testing, the IC tester also requires a fine resolution that is much smaller than the tester clock period and a time delay adjustment range for both drive and strobe actions that is larger than the tester clock period. Conceptually, this requirement is illustrated in Figures 4A and 4B. Figure 4B shows two different timing verniers A and B, each referenced

to the tester clock edge of Figure 4A. The timing vernier A has a delay ΔVa which is smaller than the tester clock period T. The timing vernier B has a delay NT+ΔVb which is larger than the tester clock period T.

(8) The paragraph from page 8, line 11 to page 8, line 17 has been amended as follows:

Figure 5 is a circuit diagram showing an example of structure in the vernier delay unit 14 for generating the timing verniers shown in Figure 4B. The vernier delay unit 14 allows delay in timing vernier data over many tester clock periods, with the resolution ~~of~~ equal to the fine vernier timing resolution, i.e., a fraction of the tester clock period.

(9) The paragraph from page 8, line 11 to page 8, line 17 has been amended as follows:

The vernier delay unit <u>14</u> in Figure 5 includes an adder 22, a decoder 24, an AND gate 26, delay registers (D flip-flops) 31-36 and flip-flops 43-48, OR gates 62, 64, 66 and 68, and multiplexers 52, 54, 56 and 58. The vernier delay unit 14 receives the vernier data from the pattern memory and the delay value data from the multiplexer 12 in Figure 3 at the adder 22. The vernier delay unit 14 also receives the vernier enable signal and the clock <u>at the flip-flop 43</u>.

(10) The paragraph from page 11, line 8 to page 11, line 24 has been amended as follows:

In the AC parametric measurement mode, the AC measurement mode signal is high, and the counter 72 is allowed to count. The counter 72 is initialized by writing zero. When a test pattern is run, a strobe failure through the AND gate 82 increments the counter 72 by one. Thus as in Figure 2C, the strobe is continuously shifted ~~its~~ in time during the time t_1, t_2 and t_3 until the device output signal changes the logic state. During such a time period, the time shift circuit of Figure 6 produces a failure for each strobe until the edge is detected in the device output signal. Thus, a test pattern with many strobes will increment the counter 72 many times, until no more failures are found. Then the strobe delay value data [7:0] will contain the exact minimum value required to allow the test pattern to pass. The strobe delay value data [7:0] can be read to determine what the device delay times are, by comparing the AC parametric test value to the calibration value.

(11) The paragraph from page 12, line 22 to page 12, line 29 has been amended as follows:

The coarse delay circuit receives coarse timing data which is, for example, higher bits of the timing vernier from the vernier delay unit 14 or 74. The coarse delay circuit may not be necessary when the ~~terming~~ timing vernier from the vernier delay unit has a suitable delay with an intended multiple time of the clock period. The fine delay circuit

receives fine timing data which is, for example, lower bits of the timing vernier.

(12) The paragraph from page 13, line 14 to page 13, line 23 has been amended as follows:

The fine delay circuit is configured by a plurality of variable delay circuits for producing weighted small delay times. In the example of Figure 7, the fine delay circuit includes a delay unit 177 for generating a delay time equal to a 1/2 cycle of the clock signal and a delay unit 178 for generating a delay time equal to a 1/4 cycle of the clock signal. The delay unit 177 is formed of AND gates 181 and 182, a delay element 183, and an OR gate 184. Similarly, the delay circuit 178 is formed of AND gates 185 and 186, a delay element 187, and an OR gate 188.